UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/045,601	11/07/2001	Dongyun Lee	594768121US	8571

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EXAMINER
VITAL, PIERRE M

ART UNIT	PAPER NUMBER
2188	9

DATE MAILED: 01/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>07 November 2001</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-14</u> is/are pending in the application.

     4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-14</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>11/7/01</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

     a)☐ All b)☐ Some * c)☐ None of:

         1.☐ Certified copies of the priority documents have been received.

         2.☐ Certified copies of the priority documents have been received in Application No. _____.

         3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

     * See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

     a) ☐ The translation of the foreign language provisional application has been received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)   4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)   5) ☐ Notice of Informal Patent Application (PTO-152)

3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .   6) ☐ Other: .

DETAILED ACTION

1.   This Office Action is in response to Application No. 10/045,601 filed November 7,

2001. Claims 1-14 are pending in this application.

2.   The specification and the claims have been examined with the results that follow.

Specification

3.   The disclosure is objected to because of the following informalities: In the Cross

Reference to Related Applications section, the Serial Number of the related applications

is missing.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5.   Claims 1-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Leung

(US6,415,353).

As per claim 1, Leung discloses a memory bank having words that are

addressable by addresses and having multiple sections, the memory bank comprising:

a plurality of sections, each section representing a subdivision of a word of

memory [*row 0 column 0 of bank 0 stores 256-bit in the form of 8 32-bit words*; col. 8, lines 18-44],

each section having a row enable line for each row of the memory and a column enable

line for each column of the memory for enabling access to a subdivision of a word of

memory [*row address decoder activates the word line designated by output of row address multiplexer;*

column address decoder enables column address received from column address multiplexer; col. 27,

lines 38-51], each section having a section enable line for enabling access to that

section [*identified row bank and section is accessed by cache tag memory;* col. 9, lines 30-38]; for

each row of each section, row enabler logic that enables the row enable line for that row

of that section only when the section enable line for that section is enabled [*row address*

decoder activates word line designated in the designated row; col. 32, lines 28-32]; and for each

section, column enabler logic that enables a column enable line for that section only

when the section enable line for that section is enabled [*activation of CAS enables column*

address decoder which selects word in designated column address; col. 38, lines 34-37].

As per claim 2, Leung discloses the memory bank is part of a multi-port memory

device and wherein the section enable lines are enabled based on the accessing port

[*data is retired through a first port and written through a second port;* col. 21, lines 3-10].

As per claim 3, Leung discloses different rows of different sections can be

simultaneously accessed to satisfy different memory access requests [*banks can operate*

independent of each other so that parallel operations can take lace simultaneously; col. 6, lines 45-

48].

As per claim 4, Leung discloses the row and column address enable signals are buffered to accommodate row and column latencies [*row and columns addresses are buffered*; col. 14, lines 8-10; col. 30, lines 23-34].

As per claim 5, Leung discloses the memory bank includes configuration information storage for selectively enabling sections [*row and sections of DRAM are selected for writing to cache*; col. 8, lines 15-37].

As per claim 6, Leung discloses the memory bank is part of a multi-port memory device and the selective enabling of sections is on a port-by-port basis [*data is retired through a first port and written through a second port*; col. 21, lines 3-10].

As per claim 7, Leung discloses a memory bank having words that are addressable by addresses and having multiple sections, the memory bank comprising:

a plurality of sections, each section representing a subdivision of a word of memory [*row 0 column 0 of bank 0 stores 256-bit in the form of 8 32-bit words*; col. 8, lines 18-44], each word of memory being accessible via an address [*activation of CAS enables column address decoder which selects word in designated column address*; col. 38, lines 34-37], each section being selectively enabled so that only a portion of a word corresponding to enabled sections is accessible so that sections that are not enabled use less power than sections that are enabled [*activation of CAS enables column address decoder which selects word in designated column address*; *enabled sections inherently use more power than sections that are not enabled*; col. 38, lines 34-37].

As per claim 8, Leung discloses the address is divided into a row portion and a column portion and the memory bank includes a row decoder and a column decoder to selectively accesses a word of the memory bank [*RAS# and CAS# are issued to bank 0 and decoded by decoders 182 and 183*; Fig. 1; col. 11, line 64 – col. 12, line 38].

As per claim 9, Leung discloses output of the row decoder and output of the column decoder only drives sections that are enabled [*row address decoder activates the word line designated by output of row address multiplexer, column address decoder enables column address received from column address multiplexer*; col. 27, lines 38-51].

As per claim 10, Leung discloses the outputs are buffered to accommodate row and column latencies [*row and columns addresses are buffered*; col. 14, lines 8-10; col. 30, lines 23-34].

As per claim 11, Leung discloses the memory bank is part of a multi-port memory device and wherein the section enable lines are enabled based on the accessing port [*data is retired through a first port and written through a second port*; col. 5, lines 15-20].

As per claim 12, Leung discloses different rows of different sections can be simultaneously accessed to satisfy different memory access requests [*banks can operate independent of each other so that parallel operations can take lace simultaneously*; col. 6, lines 45-48].

As per claim 13, Leung discloses the memory bank includes configuration information storage for selectively enabling sections [*row and sections of DRAM are selected for writing to cache*; col. 8, lines 15-37].

As per claim 14, Leung discloses the memory bank is part of a multi-port memory device and the selective enabling of sections is on a port-by-port basis [*data is retired through a first port and written through a second port*; col. 21, lines 3-10].
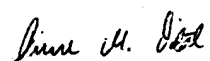
Conclusion

6.   The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111 (c) to consider these references fully when responding to this action. The documents cited therein teach memory banks having multiple sections, enabling row and columns to access words of memory.

7.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre M. Vital whose telephone number is (703) 306-5839. The examiner can normally be reached on Mon-Fri, 8:30 am - 6:00 pm, alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or

proceeding should be directed to the receptionist whose telephone number is (703) 305-

9000.

Pierre M. Vital
Art Unit 2188
January, 22 2004